What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A reference circuit comprising:

a first subcircuit, coupled to an input power source, for producing a first output voltage at a first node, said first output voltage being a function of a first threshold voltage of a first field effect transistor, a second threshold voltage of a second field effect transistor, and a first resistance of a first resistive element which is a function of a first temperature of the first subcircuit;

a second subcircuit, coupled to the input power source, for producing a second output voltage at a second node, said second output voltage being a function of a first base-to-emitter voltage of a first bipolar transistor, a second base-to-emitter voltage of a second bipolar transistor, and a second resistance of a second resistive element which is a function of a second temperature of the second subcircuit;

a summing circuit including a first control terminal coupled to said first node and a second control terminal coupled to said second node, for producing a summed power signal; and

an output circuit for outputting said summed power signal;

2. The reference circuit of claim 1, further comprising:

a coupling between a gate of said first field effect transistor, a gate of said second field effect transistor, and a drain of said first field effect transistor;

a coupling between a source of said first field effect transistor and a ground potential; and

a coupling from a source of said second field effect transistor through the first resistive element to a ground potential.

3. The reference circuit of claim 2, further comprising:

a current mirror for delivering identical currents to the first and second field effect transistors, the current mirror further comprising,

a first transistor having a source coupled to the input power source and a drain coupled to the drain of said first field effect transistor; and

a second transistor having a source coupled to the input power source and a drain coupled to the drain of said second field effect transistor.

4. The reference circuit of claim 3, wherein said first and second transistors are PMOS transistors.

5. The reference circuit of claim 1, further comprising:

a coupling between a gate of first bipolar transistor, a gate of said second bipolar transistor, and a base of said first bipolar transistor;

a coupling between an emitter of said first bipolar transistor and a ground potential; and

a coupling from an emitter of said second bipolar transistor through the second resistive element to a ground potential.

6. The reference circuit of claim 5, further comprising:

a current mirror for delivering identical currents to the first and second field effect transistors, the current mirror further comprising,

a third transistor having a source coupled to the input power source and a drain coupled to the drain of said first field effect transistor; and

a fourth transistor having a source coupled to the input power source and a drain coupled to the drain of said second field effect transistor.

7. The reference circuit of claim 6, wherein said third and fourth transistors are PMOS transistors.

8. The reference circuit of claim 1, wherein a first current which flows from the input power source through said second field effect transistor and said first resistive element to a ground potential decreases as the temperature of said first subcircuit increases.

9. The reference circuit of claim 1, wherein a second current which flows from the input power source through said second bipolar transistor and said second resistive element to a ground potential increases as the temperature of said second subcircuit increases.

10. The reference circuit of claim 1, wherein said first and second resistive elements have positive thermal coefficients.

11. A memory device comprising:

a memory array;

a control circuit;

an input/output circuit; and

a reference circuit for supplying power to the memory array, the control circuit, and the input/output circuit, said reference circuit further comprising,

a first subcircuit, coupled to an input power source, for producing a first output voltage at a first node, said first output voltage being a function of a first

threshold voltage of a first field effect transistor, a second threshold voltage of a second field effect transistor, and a temperature dependent resistance of a first resistive element;

a second subcircuit, coupled to the input power source, for producing a second output voltage at a second node, said second output voltage being a function of a first base-to-emitter voltage of a first bipolar transistor, a second base-to-emitter voltage of a second bipolar transistor, and a temperature dependant resistance of a second resistive element;

a summing circuit including a first control terminal coupled to said first node and a second control terminal coupled to said second node, for producing a summed power signal; and

an output circuit for outputting said summed power signal;

12. The memory device of claim 11, further comprising:

a coupling between a gate of said first field effect transistor, a gate of said second field effect transistor, and a drain of said first field effect transistor;

a coupling between a source of said first field effect transistor and a ground potential; and

a coupling from a source of said second field effect transistor through the first resistive element to a ground potential.

13. The memory device of claim 12, further comprising:

a current mirror for delivering identical currents to the first and second field effect transistors, the current mirror further comprising,

a first transistor having a source coupled to the input power source and a drain coupled to the drain of said first field effect transistor; and

a second transistor having a source coupled to the input power source and a drain coupled to the drain of said second field effect transistor.

14. The memory device of claim 13, wherein said first and second transistors are PMOS transistors.

15. The memory device of claim 11, further comprising:

a coupling between a gate of first bipolar transistor, a gate of said second bipolar transistor, and a base of said first bipolar transistor;

a coupling between an emitter of said first bipolar transistor and a ground potential; and

a coupling from an emitter of said second bipolar transistor through the second resistive element to a ground potential.

16. The memory device of claim 15, further comprising:

a current mirror for delivering identical currents to the first and second field effect transistors, the current mirror further comprising,

a third transistor having a source coupled to the input power source and a drain coupled to the drain of said first field effect transistor; and

a fourth transistor having a source coupled to the input power source and a drain coupled to the drain of said second field effect transistor.

17. The memory device of claim 16, wherein said third and fourth transistors are PMOS transistors.

18. The memory device of claim 11, wherein a first current which flows from the input power source through said second field effect transistor and said first resistive element to a ground potential decreases as the temperature of said first subcircuit increases.

19. The memory device of claim 11, wherein a second current which flows from the input power source through said second bipolar transistor and said second resistive element to a ground potential increases as the temperature of said second subcircuit increases.

20. The memory device of claim 11, wherein said first and second resistive elements have positive thermal coefficients.

21. A processor based system comprising:

a bus;

a processor, coupled to said bus;

an input/output device, coupled to said bus;

a memory, coupled to said bus;

wherein said memory include a reference circuit, said reference circuit further comprising,

a first subcircuit, coupled to an input power source, for producing a first output voltage at a first node, said first output voltage being a function of a first threshold voltage of a first field effect transistor, a second threshold voltage of a second field effect transistor, and a first resistance of a first resistive element which is a function of a first temperature of the first subcircuit;

a second subcircuit, coupled to the input power source, for producing a second output voltage at a second node, said second output voltage being a function of a first base-to-emitter voltage of a first bipolar transistor, a second base-to-emitter voltage of a second bipolar transistor, and a second resistance of a second

resistive element which is a function of a second temperature of the second subcircuit;

a summing circuit including a first control terminal coupled to said first node and a second control terminal coupled to said second node, for producing a summed power signal; and

an output circuit for outputting said summed power signal;

22. The processor based system of claim 21, further comprising:

a coupling between a gate of said first field effect transistor, a gate of said second field effect transistor, and a drain of said first field effect transistor;

a coupling between a source of said first field effect transistor and a ground potential; and

a coupling from a source of said second field effect transistor through the first resistive element to a ground potential.

23. The processor based system of claim 22, further comprising:

a current mirror for delivering identical currents to the first and second field effect transistors, the current mirror further comprising,

a first transistor having a source coupled to the input power source and a drain coupled to the drain of said first field effect transistor; and

a second transistor having a source coupled to the input power source and a drain coupled to the drain of said second field effect transistor.

24. The processor based system of claim 23, wherein said first and second transistors are PMOS transistors.

25. The processor based system of claim 21, further comprising:

a coupling between a gate of first bipolar transistor, a gate of said second bipolar transistor, and a base of said first bipolar transistor;

a coupling between an emitter of said first bipolar transistor and a ground potential; and

a coupling from an emitter of said second bipolar transistor through the second resistive element to a ground potential.

26. The processor based system of claim 25, further comprising:

a current mirror for delivering identical currents to the first and second field effect transistors, the current mirror further comprising,

a third transistor having a source coupled to the input power source and a drain coupled to the drain of said first field effect transistor; and

a fourth transistor having a source coupled to the input power source and a drain coupled to the drain of said second field effect transistor.

27. The processor based system of claim 26, wherein said third and fourth transistors are PMOS transistors.

28. The processor based system of claim 21, wherein a first current which flows from the input power source through said second field effect transistor and said first resistive element to a ground potential decreases as the temperature of said first subcircuit increases.

29. The processor based system of claim 21, wherein a second current which flows from the input power source through said second bipolar transistor and said second resistive element to a ground potential increases as the temperature of said second subcircuit increases.

30. The processor based system of claim 21, wherein said first and second resistive elements have positive thermal coefficients.

31. A method for supplying a reference current, comprising:

supplying a first control voltage to an summing circuit, said first control voltage being a function of a first threshold voltage of a first field effect transistor, a second threshold voltage of a second field effect transistor, and a first resistance of a first resistive element which is a function of a temperature;

supplying a first control voltage to an summing circuit, said first control voltage being a function of a first threshold voltage of a first field effect transistor, a second threshold voltage of a second field effect transistor, and a first resistance of a first resistive element which is a function of a temperature;

supplying a second control voltage to the summing circuit, said second control voltage being a function of a first base-to-emitter voltage of a first bipolar transistor, a second base-to-emitter voltage of a second bipolar transistor, and a second resistance of a second resistive element which is a function of temperature;

at a summing circuit, generating a reference current by combining a first signal and a second signal, said first signal having a gain controlled by the first control voltage on a gate of a first control transistor, and said second signal having a gain controlled by the second control voltage on a gate of a second control signal.

32. The method of claim 31, wherein said first and second resistances increase as temperature increases.

33. The method of claim 31, wherein said first control voltage is a function of the difference between the first and second threshold voltages.

34. The method of claim 33, wherein said first control voltage is also a function of the quotient of the first resistance, wherein said first resistance increases as temperature increases.

35. The method of claim 32, wherein said first control voltage increases as the temperature increases.

36. The method of claim 32, wherein said second control voltage decreases as temperature increases.